Laboratory 2

(Due date: **004/011**: Oct. 5th, **005**: Oct. 6th, **007**: Oct. 7th)

Objectives

- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

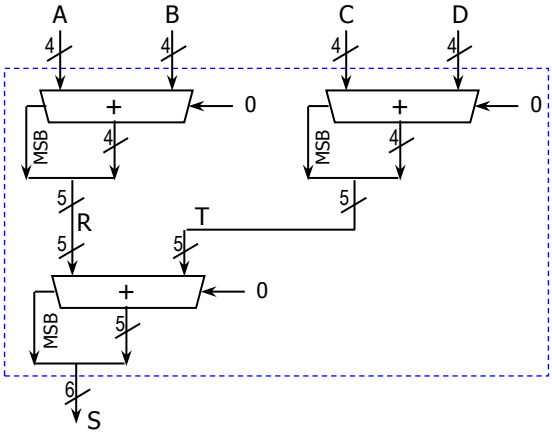
VHDL Coding

- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

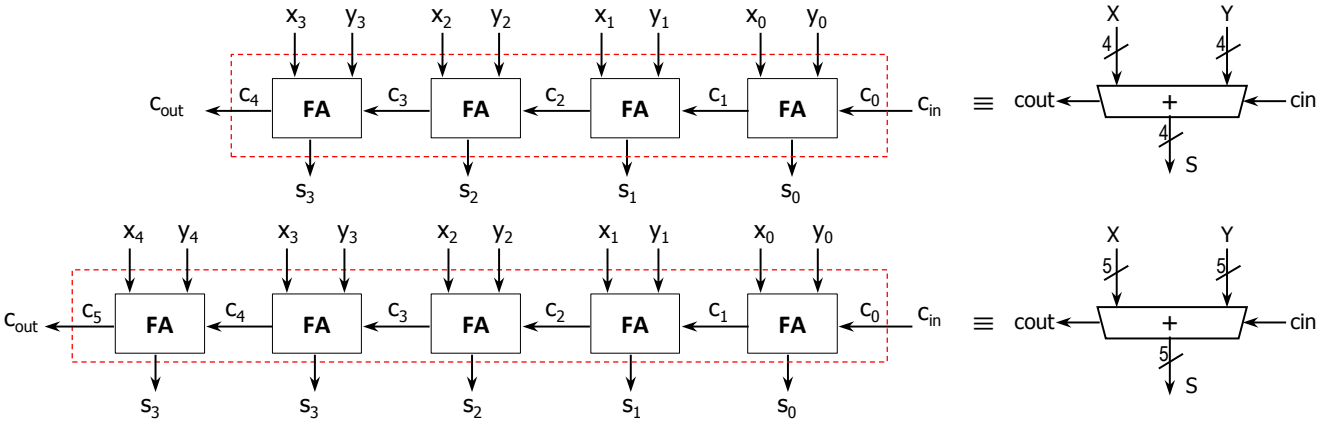
First Activity (100/100)

Design Problem

- Addition of four 4-bit unsigned numbers. The addition result requires 6 bits. This circuit can be built out of two 4-bit adders and one 5-bit adder as depicted in the figure.



- The figure below depicts the internal architecture of the 4-bit adder and the 5-bit adder. The full adder circuit is also shown.



Procedure

- **Vivado: Complete the following steps**:

  - ✓ Create a new Vivado Project. Select the corresponding Artix-7 FPGA device (e.g.: the XC7A50T-1CSG324 FPGA device for the Nexys A7-50T).

  - ✓ Write the VHDL code for the BCD Adder.
    - Use the Structural Description: Create a separate `.vhd` file for the Full Adder, the 4-bit adder, the 5-bit adder, and the top file (adder of four 4-bit numbers).

  - ✓ Write the VHDL testbench to test the circuit for the following cases:
    - **A**=0xB, **B**=0x5, **C**=0xE,**D**=0xC → **S**=101010
    - **A**=0xF, **B**=0x7, **C**=0xD,**D**=0x3 → **S**=100110
    - **A**=0xA, **B**=0x6, **C**=0x4,**D**=0x8 → **S**=011100
    - **A**=0x8, **B**=0xE, **C**=0xF,**D**=0x9 → **S**=101110

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- ✓ Perform Functional Simulation of your design. **Demonstrate this to your TA**.
  - Add the internal signals (R, T) to the waveform view. Go to: SCOPE window: testbench → UUT. Then go to Objects Window → Signal(s) → Add to Wave Window. Finally, re-run the simulation.
    - This step is extremely useful when debugging your circuit. Your circuit might be cleared of syntax errors, but there might still be errors that can be difficult to spot. By tracing the internal signals, we can determine where the error is located in the circuit.
    - For example: In this circuit, for a given set of input values, we know the expected output values and we can compute the internal signal values. Then, we compare those values with those provided by the simulation:
      - If the output S is incorrect (simulation results do not match the expected values), we then look at the value of the internal signals R and T.
        - If the values of R and T are correct (i.e., simulation results match the calculated values), then the error is located in the lower (5-bit) adder.
        - If the value of R is incorrect, then the error is on the right 4-bit adder.
        - If the value of T is incorrect, then the error is on the left 4-bit adder.
  - For the following set of inputs, complete the expected values of the listed internal signals. Then, run the simulation and compare the values in the simulation waveform with the ones you computed. This will help you figure out where the errors (if any) are located at.

A	B	C	D	R	T	S
1011	0101	1110	1100			0100
1111	0111	1101	0011			1001

- ✓ I/O Assignment: Generate the XDC file associated with your board.
  - Suggestion:

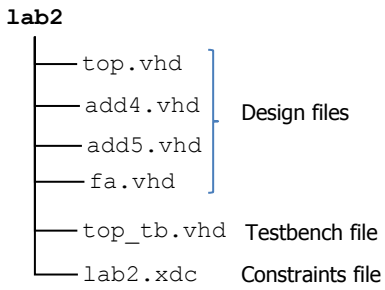
Board pin names	SW15-SW12	SW11-SW8	SW7-SW4	SW3-SW0	LED5	LED4	LED3	LED2	LED1	LED0
Signal names in code	A_3-A_0	B_3-B_0	C_3-C_0	D_3-D_0	S_5	S_4	S_3	S_2	S_1	S_0

  - The board pin names are used by all the listed boards (Nexys A7-50T/A7-100T, Basys 3, Nexys 4/DDR). The I/Os listed here are all active high.

- ✓ Implement your design (Run Implementation) and run Timing Simulation.

- ✓ Generate and download the bitstream on the FPGA, then perform testing. **Demonstrate this to your TA**.

- Submit (as a .zip file) the six generated files: VHDL code (4 files), VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.
  - ✓ Your .zip file should only include one folder. Do not include subdirectories.
  - ✓ It is strongly recommended that all your design files, testbench, and constraints file be located in a single directory. This will allow for a smooth experience with Vivado.



TA signature: _____ **Date:** _____